"gate inverse clk output" means that the output is the inverse of the clock seen on the gate; and "Cload" is an expression for capacitance load.

IN THE CLAIMS:

Please substitute the following claims for the same numbered claims in the application.

7. (Amended) The method in claim 2, wherein said modifying prevents a delay in propagation of said gating signals across said gating device from inappropriately outputting a portion of a clock pulse.

10. (Amended) The method of claim 4, wherein the computing of said setup test comprises:
computing a propagated mode test value,
computing an input-to-input test value of zero, and
using the less pessimistic of said computed test values.

14. (Amended) The method in claim 11, wherein said modifying prevents a delay in propagation of said gating signals across said gating device from inappropriately outputting a portion of said clock pulse.

21. (Amended) The program storage device in claim 18, wherein said modifying prevents a delay in propagation of said gating signals across said gating device from inappropriately outputting a portion of a clock pulse.